9. (Amended) A ferroelectric memory device comprising:

a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

C2

an interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor;

a first interconnection layer formed on the interlevel dielectric film;

an upper interlevel dielectric film formed to cover the first interconnection layer; and

a second interconnection layer formed on the upper interlevel dielectric film,

wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode; and

wherein the second interconnection layer totally covers the bottom electrode of the ferroelectric capacitor in the planar layout.

Please add the following new claim 11 as follows:

C3

--11. (New) The device of claim 8, wherein the second interconnection layer is made of a material containing at least one of aluminum and copper.--

REMARKS

At the outset, the Examiner is thanked for the review and consideration of the present application.

The Examiner's Office Action dated July 24, 2001, has been received and its contents reviewed. By this Amendment claims 1, 8, and 9 have been amended, and new claim 11 has

been added. Accordingly, claims 1-11 are pending in the present application, of which claims 1, 8, and 9 are independent.

Referring now to the Office Action, the drawings are objected to as all the features in claims 8-10 are not shown. Applicants respectfully submit that, since the Examiner did not specifically point out which particular feature of claims 8-10 is not shown in the drawing, it is presumed that the Examiner referred to the second interconnection layer. Accordingly, Applicants are submitting herewith amended Figs. 1 and 3 with amendment shown in red ink to indicate the second interconnection layer of claims 8-10. Moreover, Applicants respectfully direct the Examiner to page 12, line 22 to page 13, line 7 of the present specification for support of this amendment.

Applicants also submits herewith a letter to the Official Draftsperson requesting the approval of the correction to Figs. 1 and 3. If the Examiner is not satisfied with the amendment to Figs. 1 and 3, and if the Examiner was referring to other features in the claim, Applicants would respectfully request the Examiner to be more specific with regard to any future drawing objections.

In view of the drawing amendment, the objection to the drawings is respectfully requested to be reconsidered and withdrawn.

The specification is objected to as failing to provide adequate written description for the limitations in claims 8-10. Applicants presume that the objection was made in reference to the second interconnection layer recited in claims 8-10. As such, Applicants respectfully traverse this rejection for the reason that clear description and support for particularly the second interconnection layer of claims 8-10, can be found at least in, e.g., page 12, line 22 to page 13, line 17 of the specification of present invention.

Further, Applicants respectfully direct the Examiner to MPEP § 2163.04 (page 2100-168, August 2001), which states that a description as filed is presumed to be adequate unless or until sufficient evidence or reasoning to the contrary has been presented by the Examiner to rebut the presumption, and that the Examiner, therefore, must have a reasonable basis to challenge the adequacy of the written description, and so on ...

As discussed above, the Examiner's objection to the specification was non-specific, and Applicants have responded to the extent possible with the presumption. Accordingly, this

objection is respectfully requested to be reconsidered and withdrawn. If the Examiner wishes to maintain the objection to the specification, Applicants would respectfully request the Examiner to provide sufficient evidence or reasoning for the objection.

Claims 1-6 are rejected under 35 U.S.C. § 102(e) as anticipated by Chinu et al. (JP 11-121705A - hereafter Chinu). This rejection is respectfully traversed at least for the reasons provided below.

As amended, claim 1 further recites, among other features, dummy bit lines connected to the ferroelectric capacitor that is not used for the circuit operation. Support for this feature can be found at least in, e.g., page 12, lines 11-21 of the specification. Applicants respectfully submit that Chinu complete fails to teach, disclose, or suggest dummy bit lines. Therefore, Chinu does not anticipate amended claim 1. Accordingly, the § 102(e) rejection of independent claim 1 and its dependent claims 2-6 is respectfully requested to be reconsidered and withdrawn.

Claim 7, which depends from claim 1, is rejected under 35 U.S.C. § 103(a) as unpatentable over Chinu. This rejection is respectfully traversed for the reasons set forth above with regard to the § 102(e) rejection of independent claim 1. More particularly, Chinu fails to teach, disclose, or suggest dummy bit lines. Accordingly, the § 103(a) rejection of claim 7 is respectfully requested to be reconsidered and withdrawn.

Claims 8-10 are rejected under 35 U.S.C. § 103(a) as unpatentable over Chinu in view of Hayashi et al. (U.S. Patent No. 6,174,766B - hereafter as Hayashi). This rejection is respectfully traversed at leased for the reasons provided below.

According to amended claims 8 and 9 of the present invention, a second interconnection layer covers the top and bottom electrodes, respectively. Hence it is possible to prevent the characteristics of a ferroelectric capacitor from being deteriorated due to annealing conducted before the forming of the second interconnection. Moreover, the stress applied to the ferroelectric capacitor during the formation of the second interconnection layer can also be relaxed, as described in page 12, line 22 to page 13, line 7 of the specification.

Turning to the cited references, Chinu discloses among other things, memory cells, transistors, and a first interconnection layer. However, Applicants respectfully submit that Chinu completely fails to teach, disclose, or suggest a second interconnection layer.

Hayashi teaches a second interconnection layer that covers memory cells, according to column 13, line 44 to column 14, line 21 and Fig. 13 of Hayashi. However, Applicants respectfully submit that Hayashi completely fails to teach, disclose, or suggest the relationship of the position of the second interconnection layer and the memory cells in a planar layout, as recited in Applicants' amended claims 8 and 9.

As Chinu is deficient in a second interconnection layer, and as Hayashi is deficient in teaching, disclosing, or suggesting the positions of the second interconnection layer and the memory cells in a planar layout as recited in claims 8 and 9, their combination in the §103(a) rejection is improper. Accordingly, the rejection of claims 8 and 9 are respectfully requested to be reconsidered and withdrawn.

As claim 10 and newly added claim 11 are dependent from claims 8 and 9, respectively, claims 10 and 11 are also distinguishable over Chinu and Hayashi .

CONCLUSION

Having responded to all rejections set forth in the outstanding non-Final Office Action, it is submitted that claims 1-11 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

By _____

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VERSION OF AMENDED CLAIM WITH
MARKINGS TO SHOW CHANGES MADE

1. (Three Times Amended) A ferroelectric memory device comprising:

a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

an interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor; [and]

a first interconnection layer formed on the interlevel dielectric film[,]

a memory cell composed of the ferroelectric capacitor and the memory cell transistor; and

dummy bit lines connected to the ferroelectric capacitor that is not used for the circuit operation,

wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode;

wherein the memory cell comprises a memory cell array arranged in a matrix, and

wherein the dummy bit line is arranged at the edge of the memory cell array.

8. (Amended) [The device of claim 1, further comprising:]

A ferroelectric memory device comprising:

a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

an interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor;

a first interconnection layer formed on the interlevel dielectric film;

a second inteconnection layer formed on the upper interlevel dielectric film,

wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode; and

wherein the second interconnection layer totally covers the top electrode of the ferroelectric capacitor in the planar layout.

9. (Amended) [The device of claim 1, further comprising:]

A ferroelectric memory device comprising:

a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;

a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;

an interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor;

a first interconnection layer formed on the interlevel dielectric film;

an upper interlevel dielectric film formed to cover the first interconnection layer; and

a second interconnection layer formed on the upper interlevel dielectric film,

wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode; and

wherein the second interconnection layer totally covers the bottom electrode of the ferroelectric capacitor in the planar layout.